

PJ04N03D

25V N-Channel Enhancement Mode Field Effect Transistor

FEATURES

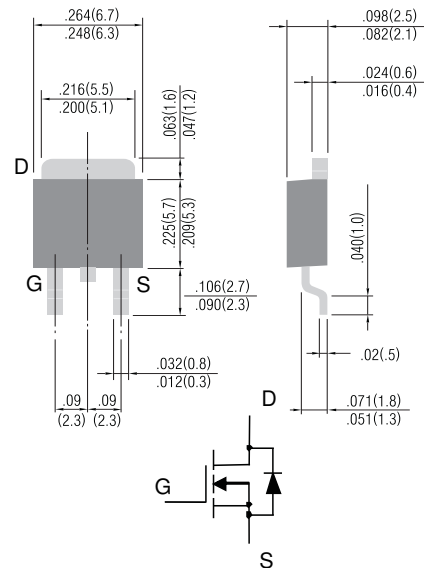
- $R_{DS(ON)}, V_{GS}@10V, I_{DS}@30A=4m\Omega$
- $R_{DS(ON)}, V_{GS}@5.0V, I_{DS}@24A=6m\Omega$
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters and Motor Drivers
- Fully Characterized Avalanche Voltage and Current
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case : TO-252 Molded Plastic
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 04N03D

TO-252

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		Symbol	Limits	Units
Drain-Source Voltage		V _{DS}	25	V
Gate-Source Voltage		V _{GS}	±20	V
Continous Drain Current	T _C =25°C	I _D	80	A
Pulsed Drain Current ⁽¹⁾		I _{DM}	220	A
Avalanche Energy L=0.1mH, I _D =53A, V _{DD} =25V		E _{AS}	140	mJ
Power Dissipation	T _C =25°C	P _D	100	W
	T _C =75°C		66	
Operating Junction and Stroage Temperature Range		T _J , T _{STG}	-55 to +175	°C
Junction-to-Case		R _{θJC}	1.5	°C/W
Junction-to-Ambient		R _{θJA}	50	

NOTE : Pulse width limited by maximum junction temperature

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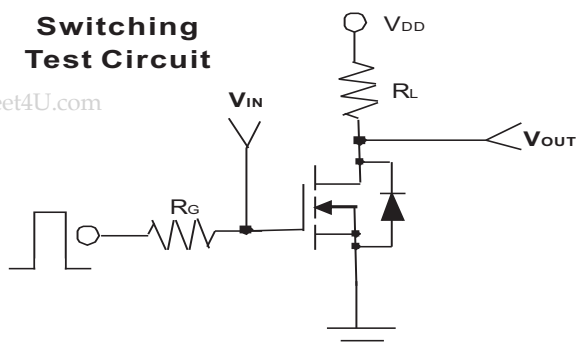
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ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, Unless Otherwise Noted)

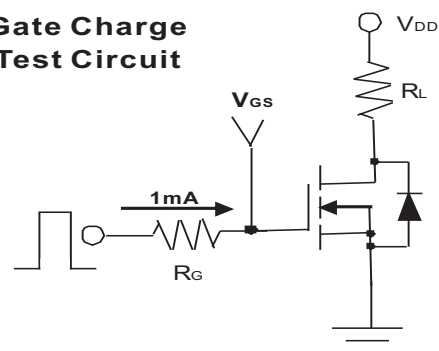
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	25	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
Drain-Source On-state Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$	-	3.6	4.0	$m\Omega$
		$V_{GS}=5V, I_D=24A$	-	4.8	6.0	$m\Omega$
Gate-Body Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=20V, V_{GS}=0V, T_J=125^{\circ}\text{C}$	-	-	25	μA
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=10V, V_{GS}=10V$	65	-	-	A
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=24A$	15	-	-	S
DYNAMIC						
Total Gate Charge	Q_G	$V_{DS}=15V, V_{GS}=5V, I_D=30A$	-	26.4	-	nC
		$V_{DS}=15V, V_{GS}=10V, I_D=30A$	-	58.2	-	nC
Gate-Source Charge	Q_{GS}	$V_{DS}=15V, V_{GS}=10V, I_D=30A$	-	5.4	-	nC
Gate-Drain Charge	Q_{GD}	$V_{DS}=15V, V_{GS}=10V, I_D=30A$	-	11.6	-	nC
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=15V, I_D=1A, V_{GS}=10V, R_{GS}=3.6\Omega$	-	17.6	22	nS
Rise Time	t_r		-	11.8	18	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48.6	72	nS
Fall Time	t_f		-	19.2	26	nS
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=15V, f=1\text{MHz}$	-	2950	-	pF
Output Capacitance	C_{oss}		-	520	-	pF
Reverse Transfer Capacitance	C_{rss}		-	430	-	pF
Gate Resistance	R_g	$V_{GS}=15\text{mV}, V_{DS}=0V, f=1\text{MHz}$	-	1.2	-	Ω
Source-Drain Diode						
Continuous Current	I_S		-	-	80	A
Forward Voltage	V_{SD}	$I_F=30A, V_{GS}=0V$	-	-	1.3	V

NOTE : Plus Test: Pluse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Switching Test Circuit

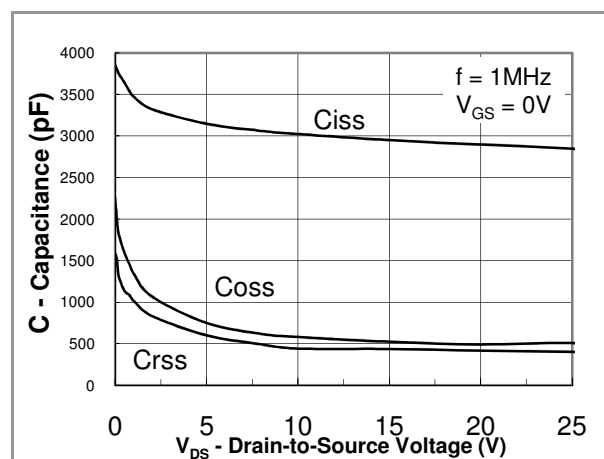
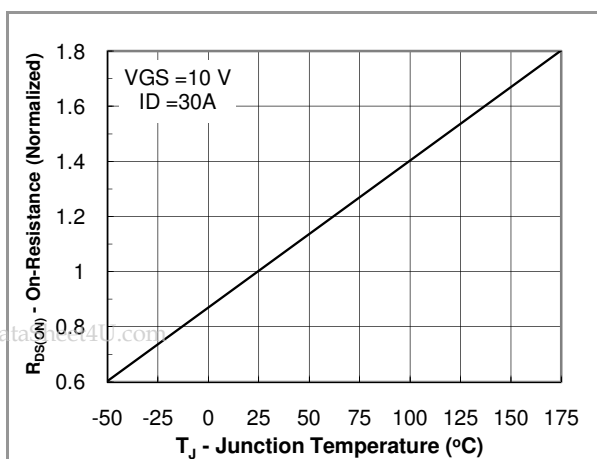
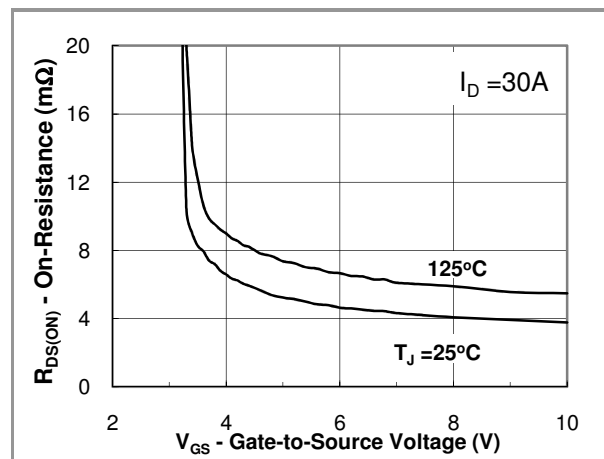
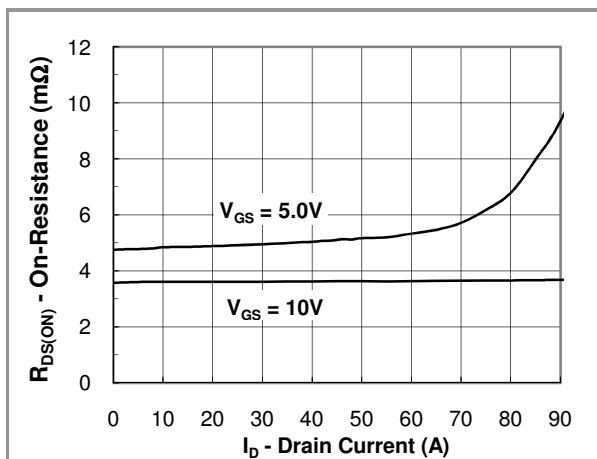
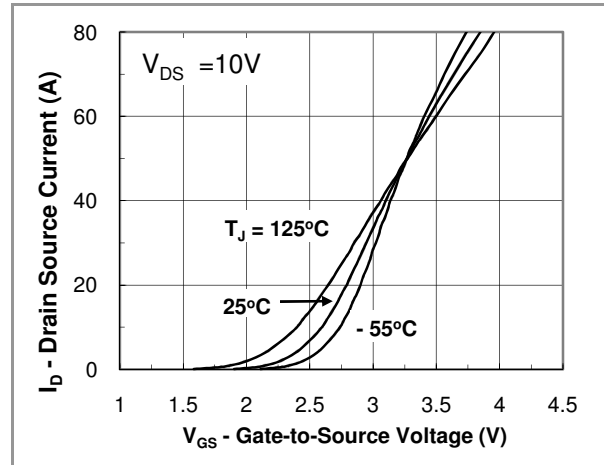
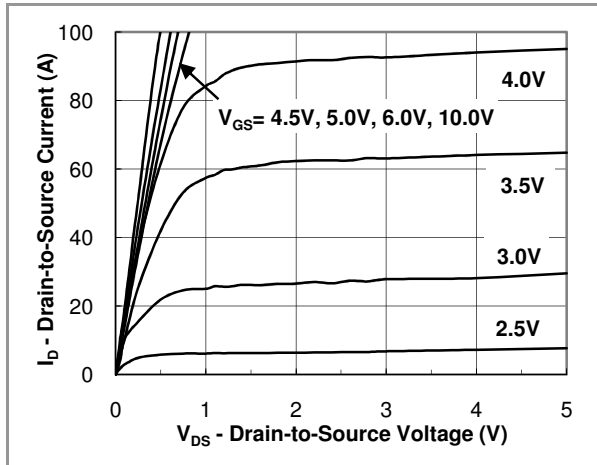


Gate Charge Test Circuit



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Typical Characteristics Curves ($T_a=25^\circ\text{C}$, unless otherwise noted)





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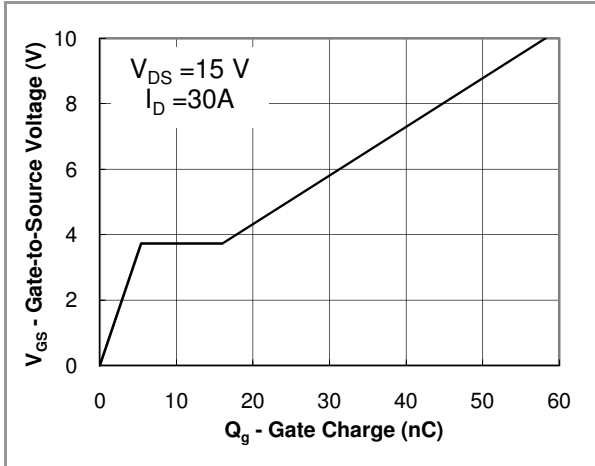


Fig. 7 Gate Charge Waveform

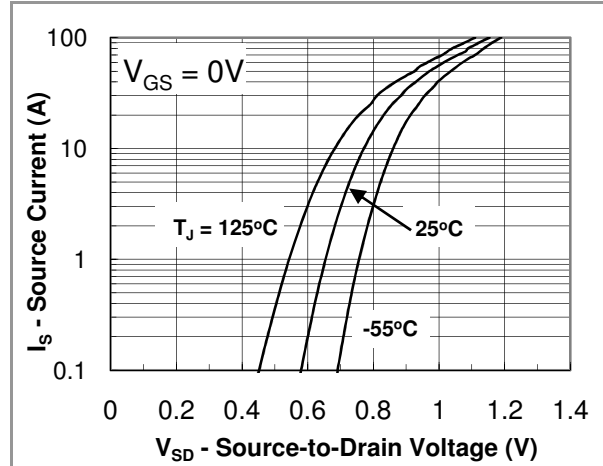


Fig. 8 Source-Drain Diode Forward Voltage

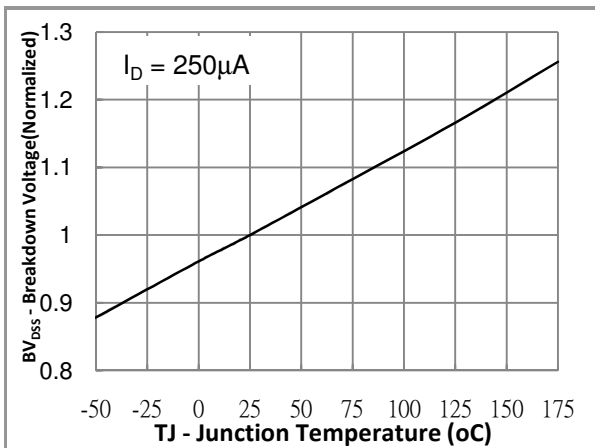


Fig. 9 Breakdown Voltage vs Junction Temperature

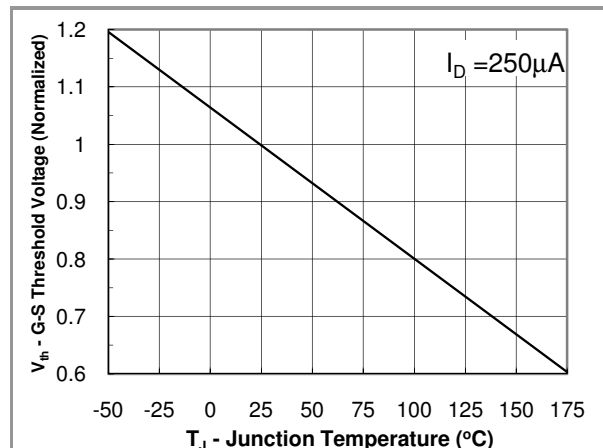
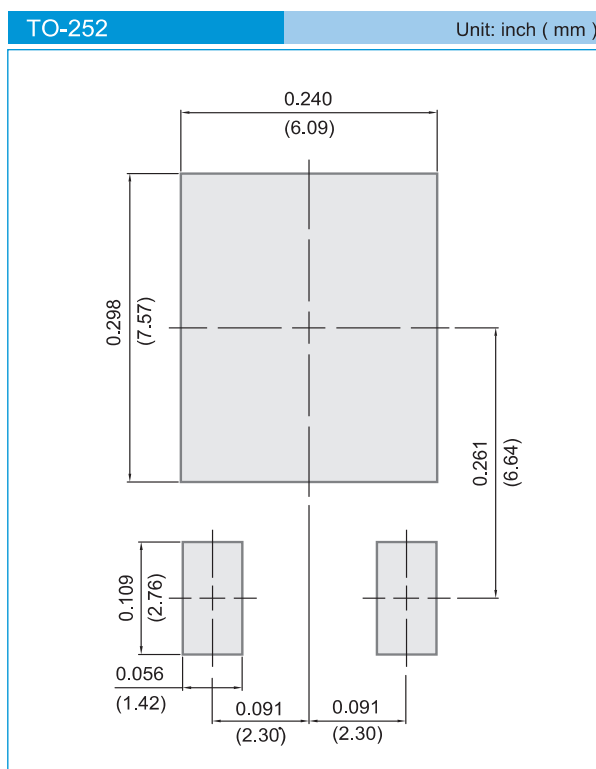


Fig. 10 Threshold Voltage vs Junction Temperature

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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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